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for a

# BUFFER AMPLIFIER ARCHITECTURE FOR SEMICONDUCTOR MEMORY CIRCUITS

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# BUFFER AMPLIFIER ARCHITECTURE FOR SEMICONDUCTOR MEMORY CIRCUITS

## BACKGROUND

### FIELD OF THE INVENTION

[0001] The present invention relates to design of semiconductor memory circuits. More particularly, it relates to a buffer amplifier architecture for buffering signals that are supplied in parallel to identical chips on a semiconductor circuit module, particularly DRAM chips on a DRAM memory module.

### BACKGROUND INFORMATION

[0002] In semiconductor memory modules, for example DRAM memory modules, which are clocked at ever higher frequencies, it is paramount that signals supplied to a group of identical chips in parallel, such as address, command and data signals, should have the same signal propagation time to the extent possible. In this context, the delay time range of registers and buffer amplifier architectures that are used in conventional semiconductor memory modules provided with registers is frequently too high. The delay time typically ranges from 0.9 ns to 2.5 ns. As a result, at frequencies above 100 mHz, the time tolerances of the signals on the command/address bus are very narrow. Typically, this has been compensated for by a register delay using an adjustable clock delay. The setting of a clock delay, once made, is then fixed and does not adapt to different characteristics of the semiconductor circuit module. The inability to change the clock delay may be undesirable in certain applications.

## SUMMARY

[0003] An exemplary embodiment of the present invention provides an architecture, applicable to buffer amplifiers and registers, that contains an adjustable delay and a fixed-delay feedback loop, which electrically encompasses the same path as the usual command and address lines. This reduces the difference between a minimum and a maximum delay from a buffer amplifier or register architecture to memory chips, and renders the delay independent of the parameters of the printed circuit board in the semiconductor circuit module.

[0004] In an exemplary embodiment of the present invention, a buffer amplifier architecture for buffering signals that are supplied in parallel to identical chips on a semiconductor circuit module includes a first set of receiver elements, designed for parallel reception of the signals, and a first set of output buffer amplifiers, each of which contains an input connected to an output of a respective receiver element in the first set of receiver elements. The first set of buffer amplifiers receives signals from the first set of receiver elements and produces buffered output signals that are supplied to chips on the semiconductor circuit module via a signal line network. The buffer amplifier architecture also includes a second set of receiver elements (also referred to as "system clock receiver elements"), designed for receiving a system clock signal, and a second set of output buffer amplifiers, each of whose input is connected to an output from a system clock receiver element, for the purpose of producing a buffered output clock signal.

[0005] In addition, a first set of delay circuits, each of which produce an adjustable delay time, is connected between the output of each of the first type of receiver

elements and the input of each buffer amplifier in the first set of buffer amplifiers. The delay circuits provide a signal delay between output from a receiver element and input to an output buffer, according to a set delay time. A second set of delay circuits with an adjustable delay time is provided between the output of a clock signal receiver element and an input of a clock signal output buffer amplifier, for the purpose of delaying the clock signal between an output from the receiver element and an input at the buffer amplifier, in accordance with a set delay time.

[0006] Additionally, a delay detector circuit is provided that contains a first and a second input, where the first input is connected to the output of the clock cycle receiver element and the second input is connected via a feedback loop to an output of the clock signal output buffer amplifier. The delay detector circuit provides for the detection of an actual delay time between a clock signal applied to its first and second inputs. A third input to the delay detector circuit applies a reference signal indicating a nominal delay. The delay detector circuit also contains a differential amplifier, which is arranged to produce a control voltage that corresponds to the difference between the detected actual delay time and the nominal delay time indicated by the reference signal. The differential amplifier control voltage is supplied to a control input on the first delay circuit, and also supplied to a control unit on the clock signal delay circuit, for the purpose of setting the delay time.

[0007] The structure and operation of the buffer amplifier architecture which have been described above, thus reduce the difference between the minimum and the maximum delay from the buffer/register to a semiconductor chip and also render the delay independent of the parameters of the printed circuit board.

[0008] The foregoing and further advantageous features of the present invention are explained in more detail in the description below with reference to the drawings.

## BRIEF DESCRIPTION OF THE DRAWINGS

[0009] Figure 1 illustrates a schematic of a buffer amplifier architecture according to an embodiment of the present invention.

[0010] Figure 2 depicts a circuit diagram of a preferred architecture of a delay detector circuit from Figure 1, according to a preferred embodiment of the present invention.

[0011] Figure 3 is a signal timing diagram showing signals at various circuit points in the delay detector circuit shown in Figure 2.

[0012] Figure 4 depicts a section of a register module according to another exemplary embodiment of the present invention.

## DETAILED DESCRIPTION OF THE INVENTION

[0013] The following list of symbols is used consistently throughout the text and drawings.

| | |
|---|---|
| 1 | Buffer amplifier architecture |
| 2 | Command-address signals |
| 3 | Clock signal |
| 4 | Reference signal |
| 51, 52 | First and second receiver elements |
| 6 | Delay detector circuit |
| 71, 72 | First, second delay circuits |
| 81, 82 | First, second output buffer amplifiers |
| 9 | Reference line network |
| 10 | Terminating capacitance elements |

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| 11 | Feedback loop |
| 12 | Signal line network |
| 13 | DRAM memory chips |
| 14, 15 | First and second input for the delay detector circuit 6 |
| 16 | Exclusive-OR gate |
| 17 | Resistor |
| 18 | Output of the exclusive-OR gate |
| 20 | Output of an integration circuit |
| 21 | Capacitor |
| 22 | Differential amplifier |
| 23 | Output of the differential amplifier 22 |
| 80 | Register |

[0014] Referring to Figure 1, a buffer amplifier architecture, denoted generally by 1, contains a first receiver element 51, in the form of a differential amplifier for receiving command and address signals 2 (Figure 1 shows one channel only, while the actual number of signals 2 is in the range from 22 to 48). A second receiver element 52, implemented as a differential amplifier, receives differential clock signals 3. An output of first receiver element 51 is connected via first delay circuit 71, having an adjustable delay time $\Delta t_{var}$, to an input on first output buffer amplifier 81, which is in the form of a push-pull buffer amplifier.

[0015] In the same manner, the output of the second receiver element 52 is connected via a second delay circuit 72, having an adjustable time delay $\Delta t_{var,}$ to an input on a second output buffer amplifier 82, which, like the first output buffer amplifier 81, is in the form of a push-pull buffer amplifier.

[0016] The respective outputs of the first output buffer amplifiers 81 are connected via a line network 12 on a printed circuit board (not shown) to command and address inputs on a plurality of parallel DRAM chips DRAM1, DRAM2, ..., DRAM5.

[0017] The output of the second output buffer amplifier 82, which carries the clock signal delayed by the second delay circuit 72 with a variable delay, is connected via a reference line network 9 on the printed circuit board (not shown) to terminating capacitance elements 10, which have the same capacitance as the signal inputs of the memory chips 13. Capacitance elements 10 can either be dummy pins on the memory chips 13 or unused signal inputs on the same. This renders the system insensitive to variations in the parameters of the memory chips 13. It is important that the topology of signal line network 12 and of the reference line network 9 are the same in electrical terms. From reference line network 9, a feedback line 11 is routed to an input 15 on a delay detector circuit 6, whose architecture and operation is described below with reference to Figures 2 and 3.

[0018] Figure 2 shows an exemplary embodiment of the present invention, which includes a circuit architecture for delay detector circuit 6. An input 14 on an exclusive-OR gate 16 receives a clock signal which is output from receiver element 52, while the other input 15 to delay detector circuit 6 is connected to feedback line 11 leading from reference line network 9.

[0019] Figure 3 shows examples of signal profiles for the two input signals 14 and 15 to exclusive-OR gate 16, as well as an output signal 18, for two different cases: 1) a long delay $\Delta t1$ (left hand side in Figure 3) and 2) a shorter delay $\Delta t2$ (right hand side in Figure 3). The length of a pulse 18 is equal to the delay in the command and

address signal network. Connected to output 18 of the exclusive-OR gate 16 is an integrator, which comprises a resistor 17 and a capacitor 21, and delivers to circuit point 20 a voltage level 20' that corresponds to the length of pulse 18 (cf. last row in Figure 3). Voltage 20' at point 20 is applied to an inverting input on a differential amplifier 22, whose noninverting input has a reference voltage indicating a nominal delay applied to it. The reference voltage, which is applied to connection 4 of delay detector circuit 6, is preferably derived from the supply voltage for exclusive-OR gate 16, for example, by a voltage divider.

[0020] An output signal 23 from differential amplifier 22 (acting as a comparator) is supplied to control inputs on delay circuits 71 and 72, for the purpose of setting their delay time. If, by way of example, the relation 1 V per 1 ns delay time ($\Delta t_{var}$) in delay circuits 71 and 72 holds true, a control voltage of 1.25 V at input 4 of the delay detector circuit 6, gives a delay time of 1.25 ns from buffer input 2, to the input of memory chips 13, for all command and address signals. If, as mentioned, the voltage at input 4 of delay detector circuit 6 is derived from the supply voltage for exclusive-OR gate 16, the delay which is set on delay circuits 71 and 72 is not dependent on the supply voltage. A phase shift between inputs 14 and 15 to delay detector circuit 6 (as a percentage of the cycle time) is determined by the voltage on input 4 (percentage of the supply voltage). The set delay time cannot be shorter than the maximum delay time in buffer amplifier architecture 1, for the case in which the delay time set on delay circuits 71 and 72 is at a minimum.

[0021] Figure 4 shows another exemplary embodiment of the present invention, in which a buffer amplifier architecture 1' is used in a register architecture. The circuit

architecture depicted in Figure 4 differs from that in Figure 1 merely by the addition of register 80, which is arranged between the output of first receiver elements 51 and the input of first delay circuits 71. Register 80 is clocked by the clock signal produced by receiver element 52 for the purpose of latching the command and address signals.

[0022] In an exemplary embodiments of the present invention, the buffer amplifier architecture depicted above can either constitute a separate integrated circuit chip on a printed circuit board, or can be integrated in another chip, for example an interface chip, on the printed circuit board.

[0023] Thus, as will be appreciated by those skilled in the art, an embodiment of the present invention provides an architecture, applicable to devices such as buffer amplifiers and registers, that contains an adjustable delay and a fixed-delay feedback loop, which electrically encompasses the same path as conventional command and address lines. This reduces the difference between a minimum and a maximum delay from a buffer amplifier architecture or a register architecture to memory chips, and renders the delay independent of the parameters of the printed circuit board in the semiconductor circuit module.

[0024] In accordance with a further aspect of the invention, the feedback loop has a reference line network having the same structure and the same electrical properties as capacitance elements that terminate the signal line network and the reference line network and have the same capacitances as the signal inputs on the chips on the semiconductor circuit module. Preferably, these capacitance elements are produced by dummy pins on the chips or by unused signal inputs on the same.

[0025] In the case of semiconductor memory modules, the signals buffered by the buffer amplifier architecture are preferably command and address signals. Preferably, the first set of receiver elements and the additional clock cycle receiver element all have respective differential amplifiers. Preferably, the first set of output buffer amplifiers and the second set of output buffer amplifier connected to the system clock receiver elements all have respective push-pull amplifiers.

[0026] The delay detector circuit preferably has an exclusive-OR gate, with the first and second inputs, and an R-C element, forming an integrator architecture at the output of the exclusive-OR gate, for the purpose of producing a voltage level that corresponds to the actual delay time, and which is supplied to an inverting input of the differential amplifier in the delay detector circuit. The reference signal applied to the third input of the delay detector circuit is preferably derived from the supply voltage for the exclusive-OR gate. In this way, the delay on the controlled delay line is independent of the supply voltage.

[0027] The buffer amplifier architecture either can be a separate integrated chip located on the printed circuit board in the semiconductor circuit module, or instead can be integrated in another chip on the semiconductor circuit module.

[0028] The foregoing disclosure of the preferred embodiments of the present invention has been presented for purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise forms disclosed. Many variations and modifications of the embodiments described herein will be apparent to one of ordinary skill in the art in light of the above disclosure. The scope

of the invention is to be defined only by the claims appended hereto, and by their equivalents.

[0029] Further, in describing representative embodiments of the present invention, the specification may have presented the method and/or process of the present invention as a particular sequence of steps. However, to the extent that the method or process does not rely on the particular order of steps set forth herein, the method or process should not be limited to the particular sequence of steps described. As one of ordinary skill in the art would appreciate, other sequences of steps may be possible. Therefore, the particular order of the steps set forth in the specification should not be construed as limitations on the claims. In addition, the claims directed to the method and/or process of the present invention should not be limited to the performance of their steps in the order written, and one skilled in the art can readily appreciate that the sequences may be varied and still remain within the spirit and scope of the present invention.